

REMARKS

Claims 1-12 are pending in this application. Claim 1 has been amended. Claim 7 has been deleted.

Claims 1 and 8 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Emesh et al. (U.S. Patent No. 5,728,603) ("Emesh"). The rejection is respectfully traversed.

The present invention relates to a method of fabricating a semiconductor device according to which an oxygen-deficient dielectric film is subjected to wet oxidation in a rapid thermal process chamber. As such, amended independent claim 1 recites a method of fabricating a semiconductor device by "depositing an oxygen-deficient dielectric film" and "subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the dielectric film." Dependent amended claim 8 recites the limitation that the dielectric film includes "a material having a dielectric constant of at least about 25."

Emesh relates to a method of forming a crystalline perovskite phase of a ferroelectric dielectric material for an integrated circuit. (Abstract). According to Emesh, "a layer of amorphous ferroelectric precursor material" is deposited on a substrate and then annealed at "a temperature sufficient to cause a phase transformation to a ferroelectric crystalline perovskite phase" in an oxidizing ambient in presence of water vapors. (Col. 3, lines 21-30). The annealing step is carried out at "a temperature below 500 °C." (Col. 3, lines 41-45). This way, "many of the problems . . . related to the relatively high temperature which is required for processing deposited ferroelectric layers to form a crystalline phase of the ferroelectric dielectric material" are avoided. (Col. 3, lines 7-14).

Emesh does not disclose the subject matter of claims 1 and 8. Emesh does not teach or suggest “a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the dielectric film,” as independent amended claim 1 recites. Emesh does not teach or suggest a wet oxidation for a dielectric material having “a dielectric constant of at least about 25” (claim 8) which “increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the dielectric film” (claim 1). Emesh is silent about any diffusion of “an oxidizing species . . . through the dielectric film into a layer underlying the dielectric film,” as independent amended claim 1 recites. Because Emesh does not disclose the limitations of the claims 1 and 8, the present invention is not anticipated under 35 U.S.C. § 102 (b).

Claims 1-6, 9 and 12 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Miner et al. (U.S. Patent No. 6,114,258) (“Miner”). The rejection is respectfully traversed.

Miner relates to a method of forming an oxide in the presence of a nitrogen-containing material. (Col. 2, lines 34-35). According to Miner, a nitrogen-containing material/ nitride film 110 is first deposited over a semiconductor substrate 100. (Col. 4, lines 31-34; Figure 2). Subsequently, the substrate 100 undergoes a reoxidation process at the end of which a silicon oxide ( $\text{SiO}_2$ ) layer 120 is formed between the nitrogen-containing material/ nitride film 110 and the substrate 100. (Col. 4, lines 48-56; Figure 3). This way, the presence of nitrogen in the nitrogen-containing material/ nitride film 110 acts as “an effective barrier layer to prevent the migration of dopants, such as boron, through oxide layer 120.” (Col. 4, lines 56-59).

Miner does not disclose the limitations of the claimed invention. Miner does not disclose “subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse

through the dielectric film into a layer underlying the dielectric film,” as independent amended claim 1 recites. Miner does not increase the oxygen content of the nitrogen-containing material/ nitride film 110, which would arguably correspond to the dielectric film of the claimed invention, by subjecting the nitrogen-containing material/ nitride film 110 to a wet oxidation process. Rather, Miner oxidizes the surface of the substrate to form a new silicon oxide ( $\text{SiO}_2$ ) film 120. (Figures 2-3). Accordingly, Miner does not disclose the limitations of the claimed invention and the present invention is not anticipated under 35 U.S.C. § 102 (e).

Claims 2-3 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Emesh et al. (U.S. Patent No. 5,728,603) (“Emesh”). The rejection is respectfully traversed.

Claims 2-3 of the present invention would not have been obvious over Emesh. Each of these claims depend on claim 1 and, as noted above, Emesh does not teach or suggest the subject matter of claim 1. Accordingly, Emesh also fails to teach or suggest the subject matter of claims 2 and 3. Moreover, Emesh does not teach or suggest a wet oxidation process at “a temperature in a range of about 750 °C to about 950 °C,” as dependent claim 3 recites. There is no teaching or suggestion, therefore, for the subject matter of claims 2 and 3 and withdrawal of the rejection of claims 2 and 3 is respectfully requested.

Claim 4 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over Emesh et al. (U.S. Patent No. 5,728,603) (“Emesh”) in view of Wolf (Silicon Processing in the VLSI Era, vol. 1) (“Wolf”). The rejection is respectfully traversed.

Claim 4 depends on claim 1 and is, therefore, allowable for at least the reasons given for the allowance of claim 1. Claim 4 further recites a wet oxidation process “carried out for a duration in a range of about 20 to about 60 seconds.” Emesh expressly notes that “the initial focus of [the application] was a reduction of the crystallization temperature . . . from ~650°C. to < 500°C,” (Col. 5, lines 50-54), and a need for eliminating the

problems “related to the relatively high temperature which is required for processing deposited ferroelectric layers.” (Col. 3, lines 9-13). Thus, Emesh contains no teaching or suggestion for a wet oxidation processed for the claimed duration. Wolf also fails to teach or suggest a wet oxidation for the claimed duration. Accordingly, there is no suggestion or motivation for one skilled in the art to modify Emesh to arrive at the claimed invention and withdrawal of the rejection of claim 4 is requested.

Claims 1, 3, 4, 9-10 and 12 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Jeng (U.S. Patent No. 5,661,072) (“Jeng”). The rejection is respectfully traversed.

Jeng relates to a method for reducing oxide thinning which typically results from the oxidation of a Kooi nitride, which is defined in the semiconductor industry as a nitride region formed along the boundary of a field oxide and of a substrate. (Abstract; Col. 1, lines 29-32). According to Jeng, a pad oxide 10 “comprising a first concentration of nitrogen 14” is formed over a substrate 12. (Col. 2, lines 55-61; Figures 1-3). Although in Figures 1-3 of Jeng the oxide layer 10 and the nitrogen layer 14 are shown as three distinct layers, “layers 10 and 14 are preferably formed as a single layer.” (Col. 2, lines 61-64). After the patterning of the nitridized pad oxide 10 for the formation of field oxide regions 30, Kooi nitride regions 32 are also formed, as illustrated in Figures 2-3. (Col. 3, lines 7-40). The nitridized pad oxide 10 and the Kooi nitride regions 32 are subsequently oxidized to grow the gate oxide 40. (Col. 3, lines 55-57; Figure 4). The gate oxide 40 “can be grown using an initial-dry oxidation (O<sub>2</sub>); a Trans-LC oxidation; a wet oxidation with Trans-LC (O<sub>2</sub>/H<sub>2</sub>); and a final dry oxidation.” (Col. 3, lines 57-61).

Claims 1, 3, 4, 9-10 and 12 would not have been obvious over Jeng. First, Jeng does not disclose or suggest the step of “subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the dielectric film,” as independent amended claim 1 recites, or “at a temperature on a range of

about 750 °C to about 950 °C, as dependent claim 3 recites. Jeng discloses temperatures between about 900 °C and about 1100 °C, but these temperatures relate to the formation of a conventional field oxide region, and not to the wet oxidation of a dielectric material to increase its oxygen content. Second, Jeng does not teach, disclose or suggest “a wet oxidation in a rapid thermal process chamber,” as independent amended claim 1 recites.

Rather, Jeng teaches a four-step process for growing a gate oxide layer by “using an initial-dry oxidation (O<sub>2</sub>); a Trans-LC oxidation; a wet oxidation with Trans-LC (O<sub>2</sub>/H<sub>2</sub>); and a final dry oxidation.” (Col. 3, lines 57-61). Accordingly, the claimed invention is not obvious over Jeng and withdrawal of the rejection of claims 1, 3, 4, 9-10 and 12 is respectfully requested.

Claims 1-2, 5-6 and 9-11 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takemura (U.S. Patent No. 5,534,716) (“Takemura”). The rejection is respectfully traversed.

Takemura relates to a semiconductor device using a thin film transistor (TFT) mounted on an insulating substrate which can be utilized in a matrix type liquid crystal displaying unit. (Col. 1, lines 11-16). For this, Takemura teaches the addition of specific metal elements to a silicon film to promote its crystallization. (Col. 2, lines 57-59). In one of Takemura’s embodiments, an amorphous silicon film 303 is formed over a silicon oxide film 302, so that a nickel film 305 is sputtered by using a silicon oxide mask 304. (Col. 10, lines 22-39; Figure 7A). The substrate is placed in “an oxygen atmosphere containing 10% of steam at 550 °C to 650 °C., typically 600 °C. for 3 to 5 hours under 1 atm,” so that silicon oxide layers 312 and 313 are formed over active layer regions 310. (Col. 10, lines 53-60; Figure 7C).

Claims 1-2, 5-6 and 9-11 would not have been obvious over Takemura. Takemura does not disclose or suggest the step of “subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the

dielectric film,” as independent amended claim 1 recites. In Takemura, no dielectric film undergoes wet oxidation to increase its oxygen content. The only layers in Takemura formed in an oxygen atmosphere are silicon oxide layers 312 and 313 of Figure 7C, but these layers are formed by oxidizing the surface of the active layer, (Col. 10, lines 53-57), and not by oxidizing “an oxygen-deficient dielectric film,” as in the claimed invention. Further, the silicon oxide layers 312 and 313 of Figure 7C are not subjected to a wet oxidation to increase their oxygen content. If anything, these layers undergo an anneal step to remove the hydrogen in the silicon oxide layers. (Col. 10, lines 62-65). Thus, the claimed invention is not obvious over Takemura and withdrawal of the rejection of claims 1-2, 5-6 and 9-11 is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: March 21, 2001

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &  
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 828-2232

Attorney for Applicants

Version with markings to show changes made

1. (amended) A method of fabricating a semiconductor device, the method comprising:

~~depositing an oxygen-deficient dielectric film; and~~

subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature of at least about 450 °C and for a duration which increases [to increase] the oxygen content of the dielectric film but does not allow an oxidizing species to diffuse through the dielectric film into a layer underlying the dielectric film.